

ABSTRACT

A pulse-width controller (1800) is described. Pulse generators (1700L, 1700H) are coupled to receive clock signals (1320, 1321) and configured to extend respective high-time and low-time pulse widths to provide signals with lengthened pulse widths (1320P, 1321P). Control signals (1803, 1804) are generated from pulse-width lengthened signals (1320P, 1321P). Clock signals (1320, 1321) and the pulse-width lengthened signals (1320PB, 1321P, 1321PB) are provided to differential logic (1823 through 1828), such as Differential Cascode Voltage Switch Logic, to provide a differential output (1611, 1612) which is duty-cycle adjusted. The control signals (1803, 1804) in combination with the pulse-width lengthened signals (1320PB, 1321P, 1321PB) are used to selectively activate a respective portion of the differential logic (1823 through 1828) to pass signals to the differential output (1611, 1612).